

Please amend the paragraph beginning at line 7 on page 3 as follows:

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C2 In the cross-sectional view showing mainly the structure of a cylindrical storage node 105b, the cylindrical storage node 105b has a cylindrical portion in which an inner wall and an upper surface of a bottom portion are roughened. Numeral 109 designates a bit line formed in contact with the other source/drain region 101a between the adjacent source/drain regions. Other reference numerals designate the same or corresponding part shown in Figure 6. The reason why an outer wall of the cylindrical portion of the cylindrical storage node 105b is not roughened in the semiconductor device shown in Figure 7, is to eliminate a disadvantage that when a heat treatment is conducted with use of a silane gas to obtain a roughened surface, spherical silicon grains having [an] a uniform grain size are formed in the outer wall, and [there causes] short circuit between adjacent storage nodes are caused. Further, there is another disadvantage that the formation of the silicon grains having [an ununiform] a uniform grain size influences the formation of the dielectric film 106 and the cell plate 107 which are conducted subsequently.

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Please amend the paragraph beginning at line 8 on page 4 as follows:

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C3 In the conventional semiconductor device shown in Figure 7, it was difficult to control the size of the silicon grains formed to obtain a roughened surface, and scattering of the silicon grain size was large whereby it [use] was difficult to form a roughened surface in the cylindrical portion of the cylindrical storage node 105b.

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#### REMARKS

This Supplemental Preliminary Amendment is being filed in order to supply the U.S. Patent and Trademark Office with a marked-up version and a clean version of the specification as amended in the Preliminary Amendment filed on April 13, 2001.